IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Dureseti CHIDAMBARRAO, *et. al.*

Docket No.: FIS920030186US1

Serial No.: 10/667,601

Group Art Unit: 2812

Filed: September 23, 2003

Examiner: KENNEDY, Jennifer M.

For: **IMPROVED NFETs USING GATE INDUCED STRESS MODULATION**

U.S. Patent and Trademark Office
Customer Window, Mail Stop: Amendment
Randolph Building
Alexandria, VA 22314

AFFIDAVIT UNDER 37 C.F.R. § 1.131

Sir:

We, Dureseti Chidambarrao, Omer H. Dokumaci and Oleg G. Glushenkov do hereby declare:

1. We are co-inventors of the subject matter disclosed and recited in independent claims 1 and 16 of the above-identified application.

2. We completed the invention of claims 1 and 16 (and those claims dependent thereon) in the United States before July 17, 2003, as evidenced below.

CONCEPTION

3. Before July 17, 2003, we conceived of a method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer.

4. An embodiment of the invention, as described above, is evidenced by IBM Invention Disclosure FIS8-2003-0053 (hereinafter referred to as Athe Invention Disclosure@) attached hereto as Exhibit A. The Invention Disclosure is a copy of and is identical to the original, except that all pertinent dates have been removed therefrom.

5. All dates removed from the Invention Disclosure attached hereto are before July 17, 2003.

6. As evidenced in the attached Invention Disclosure, the method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer includes:

A. covering the p-type transistor with a mask; and

B. oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor.

7. The benefits and features of the method are shown and described in the Invention Disclosure.

8. These features and others are exemplified in the Invention Disclosure.

DUE DILIGENCE

9. Inventors Dureseti Chidambarrao, Omer H. Dokumaci and Oleg G. Glushenkov communicated with IBM patent counsel in preparing a patent application based on the Invention Disclosure prior to May 23, 2003. IBM patent counsel forwarded the Invention Disclosure to Counsel at McGuireWoods.

10. We worked diligently on the preparation of the patent application with Counsel at McGuireWoods until a final draft patent application was completed to our satisfaction. For example, communications took place between the inventors and Counsel at McGuireWoods on July 4, 2003 and

July 7, 2003. These communications included draft applications for our review. A final draft of the application was forwarded to us by Counsel at McGuireWoods on or about August 7, 2003 for our final review and approval.

11. The final draft of the patent application was filed in the U.S. Patent Office on September 23, 2003.

12. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dureseti Chidambarrao — Date

Omer H. Dokumaci — 02/10/05 — Date

Oleg G. Glushenkov — Date

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Dureseti Chidambarrao — Date: 2/9/05

Omer H. Dokumaci — Date:

Oleg G. Glushenkov — Date: 2/10/05

O.G.

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